



United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/664,856	09/19/2000	Kazuhiro Hashimoto	197372US2	5426
22850	7590 09/22/2005		EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			HUYNH, KIM T	
			ART UNIT	PAPER NUMBER
	•	•	2112	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<u>,</u>						
/	Application No.	Applicant(s)				
Office Action Summary	09/664,856	HASHIMOTO, KAZUHIRO				
Office Action Summary	Examiner	Art Unit				
The MAN INC DATE of this communication com	Kim T. Huynh	2112				
Period for Reply	The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).						
Status						
1) Responsive to communication(s) filed on <u>05 Ju</u>	Responsive to communication(s) filed on <u>05 July 2005</u> .					
,	This action is FINAL . 2b)⊠ This action is non-final.					
· — · · ·						
closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213.						
Disposition of Claims						
4)⊠ Claim(s) <u>1-23 and 27-29</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6) Claim(s) 1-23 and 27-29 is/are rejected.						
7) Claim(s) is/are objected to. 8) Claim(s) are subject to restriction and/or	r election requirement.					
of Chairman and Ch	orocas requirement					
Application Papers						
9) The specification is objected to by the Examiner.						
10)⊠ The drawing(s) filed on 19 September 2000 is/a						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.						
·	unimon rote the attached conce					
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).						
a)⊠ All b)□ Some * c)□ None of: 1.⊠ Certified copies of the priority documents have been received.						
1. Certified copies of the priority documents have been received.2. Certified copies of the priority documents have been received in Application No						
3. Copies of the certified copies of the priority documents have been received in this National Stage						
application from the International Bureau (PCT Rule 17.2(a)).						
* See the attached detailed Office action for a list of the certified copies not received.						
Attachment(s)						
1) Notice of References Cited (PTO-892) A) Interview Summary (PTO-413) Paper No(s)/Mail Date						
2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)	3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) 5) Notice of Informal Patent Application (PTO-152)					
Paper No(s)/Mail Date 6)						

Application/Control Number: 09/664,856 Page 2

Art Unit: 2112

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the request filed on 5th of July 2005 for a request for continued examination (RCE) under 37 CFR 1.114 based on the application No. 09/664,856, which the request is acceptable and an RCE has been established. Currently, claims 1-23 and 27-29 are pending in this application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-23, 27-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Thekkath et al. (US Patent 6,604,159)

As per claims 1, 8 and 15, 21-23, Thekkath discloses a data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

• A data bus (fig.6, 610 ie data bus) connected to a peripheral apparatus, said data bus having a plurality of unit data buses (fig.6, 610, col. 5, 25-36,

ie data bus comprises data lines each data line correspond to particular bus master) each of which transfers concurrently; (col.8, lines 2-15)

- A plurality of bus masters(fig.6, 601-602 ie bus masters) configured to send a request signal requesting a use of each of said unit data buses and to use said unit data buses requested when a request by means of said request signal is granted; and (col.4, lines 12-25)
- one bus controller (fig.6, 650 ie bus arbiter) connected to each of the unit
 data buses and configured to spit-control said unit data buses for said
 plurality of bus masters by giving a grant signal to the bus masters which
 grants the use of each of said unit data buses in accordance with said
 request signal wherein (col.4, lines 12-25)
- The request signal has a field comprising a plurality of bits, each of said
 plurality of bits corresponding to a respective one of said unit data buses
 and said bus controller grants the use of each of said unit data buses
 specified by the bits of said request signal. (col.8, line 38-col.9, line 25 ie
 transaction ID associated with request which corresponds to each data
 line)

As per claims 2, 9 and 16, Thekkath discloses wherein said bus controller sends the grant signal to said bus masters a bus release requesting signal requesting release of said unit data buses. (col.4, lines 12-25)

Application/Control Number: 09/664,856

Art Unit: 2112

As per claims 3, 10 and 17, Thekkath discloses wherein said bus controller includes a monitor circuit for monitoring availability of said unit data buses. (col.4,lines 12-25)

As per claims 4, 11 and 18, Thekkath discloses wherein said bus controller judges whether said unit data buses of said data bus are available based on a monitoring result of said monitor circuit, and when said unit data buses are available, said bus controller provides the grant signal of the use of said unit data buses to said bus master. (col.4, lines 12-25)

As per claims 5, 2 and 19, Thekkath discloses wherein said bus controller sends a state signal indicating the availability of said unit data buses to each of said bus masters based on a monitoring result of said monitor circuit. (col.4, lines 12-25)

As per claims 6, 13 and 20, Thekkath discloses wherein said request signal includes information specifying each unit data bus in said data bus. (col.8, line 38-col.9, line 25 ie transaction ID specifying information for each data unit)

As per claims 7 and 14, Thekkath discloses wherein said request signal includes information specifying the number of the unit data buses in said data bus. (col.8, line 38-col.9, line 25 ie transaction ID specifying information for each data unit)

As per claims 27-28, Thekkath discloses bus controller broadcasts a bus master selection signal to all of said bus masters along with said grant signal, said selection signal indicating a bus master by which said grant signal is to be received.(col.4, line 12-25)

Page 5

Application/Control Number: 09/664,856

Art Unit: 2112

As per claim 29, Thekkath discloses a data transfer control circuit for carrying out data transfer by using a plurality of bus masters, comprising:

- A data bus (fig.6, 610 ie data bus) connected to a peripheral apparatus,
 said data bus having a plurality of unit data buses(fig.6, 610, col. 5, 25-36,
 ie data bus comprises data lines each data line correspond to particular bus master), each of which transfers data concurrently; (col.8, lines 2-15)
- A plurality of bus masters (fig.6, 601-602 ie bus masters) connected to
 each of the unit data buses and configured to send a request signal
 requesting a use of each of said unit data buses, and to use said unit data
 buses requested when a request by means of said request signal is
 granted; and(col.4, lines 12-25)
- One bus controller (fig.6, 650 ie bus arbiter) connected to all of the bus
 masters and configured to split-control said unit data buses for said
 plurality of bus masters by giving a grant signal to the bus masters, which
 grants the use of each of said unit data buses in accordance with said
 request signal, wherein (col.4, lines 12-25)
- The request signal has a field comprising a plurality of bits, each of said plurality of bits corresponding to a respective one of said unit data buses, and(col.8, line 38-col.9, line 25 ie transaction ID associated with request which corresponds to each data line)
- Said bus master sends the request signal to another bus master and the bus controller, and the other bus master determines the availability of

Art Unit: 2112

each of the unit data buses based on the request signal to send the request signal specifying available unit data bus.(col.4, line 12-25)

Response to Amendment

4. Applicant's amendment filed on 7/5/05 have been fully considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571)272-3635 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 9.00AM- 6:00PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached at (571)272-3676 or via e-mail addressed to [rehana.perveen@uspto.gov].

The fax phone numbers for the organization where this application or proceeding is assigned are (571)273-8300 for regular communications and After Final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-2100.

Kim Huynh

September 18, 2005

Mark Donas

Khanh Dang